REMARKS

Claims 2, 10, 23, and 26 have been cancelled without prejudice or disclaimer, and new claims 32-35 have been added. Claim 1 and 7 stand rejected as being anticipated by Staffiere, and claims 1-31 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Scott in view of Ozawa. These rejections are respectfully traversed.

The Declaration submitted under 37 C.F.R. 1.131 is hereby withdrawn. The Applicants note that the Examiner is imposing a requirement for "exhibits, drawings or records, or photocopies" that is simply not present in 37 C.F.R. 1.131, which clearly states that the absence of such materials can be satisfactorily explained. The withdrawn Declaration identifies that the Inventor conceived of the invention in December 1997, and fabricated an experimental printed circuit board in January 1998. This Declaration was submitted to overcome Staffiere, filed on January 28, 1998. As such, it is the date of conception and not the experimental printed circuit board that is being relied upon to overcome Staffiere, and no "exhibits, drawings or records, or photocopies" of the inventor's thought processes could possibly exist. However, the Examiner has clearly shown that regardless of whether the inventors can establish that their invention was conceived prior to January 1998, that he will reject the claims on other grounds. As such, the Declaration is withdrawn.

Scott in view of Ozawa fails to provide a prima facie basis for the rejection of claims 1, 3-9, 11-22, 24, 25, and 27-35, as they fail to disclose each element of the claimed invention. The Examiner states in regards to Ozawa that "the PCB inherently comprises a via for the purpose of coupling components on opposite sides of the substrate." However, the Examiner misstates the doctrine of inherency, which requires that the missing element **necessarily** be present or inherent in **the anticipating reference**. Not only does Ozawa fail to disclose the concept of a via in any manner whatsoever, or to even use the term "via," it discloses that the board is a "wiring board," and not a printed circuit board. As insulated wires could readily be routed around the edges of the wiring board, a via is not necessarily present or inherent in Ozawa.

Furthermore, the Examiner has failed to address the fact, previously argued, that Ozawa fails to disclose a high voltage application, and furthermore, teaches away from such use, as it describes capacitors for use in wiring board circuits, which are low voltage applications. Ozawa states that it "is conceivable to replace the aforementioned dielectric substrate 2, which is made of a mixture of dielectric powder and resin, by a substrate made of glass fiber which is impregnated with a mixture of dielectric powder and resin. Through an experiment, however, it has been proved that such a material is unpreferable," due to the lower value of the dielectric constant. This teaching relates directly to a focus on increasing the value of the capacitance, and not the voltage withstand capacity or dielectric strength, which is a material property of the material that is not related to the material's dielectric constant. In contrast, the specification of the pending application discloses at page 12, lines 9-10 that it "is noted that the dielectric properties of a fiberglass printed circuit board are well suited to the formation of capacitors for high voltage applications." Although this discussion is presented to demonstrate to the Examiner that Ozawa teaches away from the use of a circuit board capacitor as a high voltage isolation barrier, this limitation has been explicitly added to claim 4 so as to prevent the Examiner from dismissing this as an argument that relies on teachings from the specification that are not contained within the claims. However, the focus here is not on the construction of the claims, but on the teachings of Ozawa, which lead one of ordinary skill in the art away from any consideration of using a circuit board capacitor as a high voltage isolation barrier, and thus apply to each claim and not just to claim 4.

Finally, claim 1 has been amended to include limitations disclosed at page 10 of the specification of the pending application, including that the high voltage isolation barrier is formed of a plurality first and second electrodes that are shaped and located so as to utilize otherwise unused portions of the surfaces of the substrate. There is absolutely no disclosure of such a plurality of first and second electrodes that are located so as to utilize otherwise unused portions of the surfaces of the substrate in Ozawa.

New claims 32-35 are drawn to exemplary embodiments that are unquestionably not disclosed by Ozawa, nor would there be any motivation to combine Ozawa with other references to provide such features. For example, claim 32 includes "a first electrode disposed on the first side of the substrate; a second electrode disposed on the second side of the substrate; a third electrode disposed within the substrate; a first conductive via through the substrate and the third electrode connecting the first electrode and the second electrode and including a high voltage isolation barrier between the first conductive via and the third electrode." Ozawa not only fails to disclose any such configuration, but the use of a high voltage isolation barrier for a conductor in a via would simply be foreign to integrated circuit design, as the operating voltages of such integrated circuits are strictly low voltage. The use of such a design to provide a high voltage isolation barrier is foreign to the design concepts and constraints of the prior art.

In regards to the Examiner's construction of Ozawa anticipating claims 17, 24 and 31, it is noted that claim 17 includes the "data access arrangement of claim 8, the first electrode being formed on a **plurality of substrates**." Claim 24 includes the "method of claim 23, the step of forming a first electrode further comprising forming the first electrode on the sides of **more than one substrate**." Claim 31 includes the "computer system of claim 29, wherein the circuit board is a multi-layer circuit board having a plurality of substrates, the first electrode being formed on **more than one substrate**." In contrast, the Examiner states that multiple substrates are "either side of substrate 6" of Ozawa. How can a "plurality of substrates" or "more than one substrate" be reasonably construed as either side of a single substrate? They cannot. Would the Examiner be satisfied being paid with a $10 bill on a $20 debt with the argument that, since the $10 bill has two sides, it is actually two $10 bills? Undoubtedly not, and this example demonstrates that this rejection is improper. Withdrawal of the rejection is requested.

CONCLUSION

In view of the foregoing remarks and for various other reasons readily apparent, Applicants submit that all of the claims now present are allowable, and withdrawal of the rejection and a Notice of Allowance are courteously solicited.

If any impediment to the allowance of the claims remains after consideration of this amendment, a telephone interview with the Examiner is hereby requested by the undersigned at (214) 939-8657 so that such issues may be resolved as expeditiously as possible.

A response to the pending office action within the one month extension of time was due on April 25, 2005. Accordingly, this Request for Continued Examination is timely filed within the one month extension period on May 25, 2005. An additional fee of $120 for a one month extension of time is believed to be due, and the Commissioner is hereby authorized to charge that fee to the deposit account of Godwin Gruber LLP, No. 50-0530. If any applicable fee or refund has been overlooked, the Commissioner is hereby authorized to charge any fee or credit any refund to the deposit account of Godwin Gruber LLP, No. 50-0530.

Respectfully submitted,

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